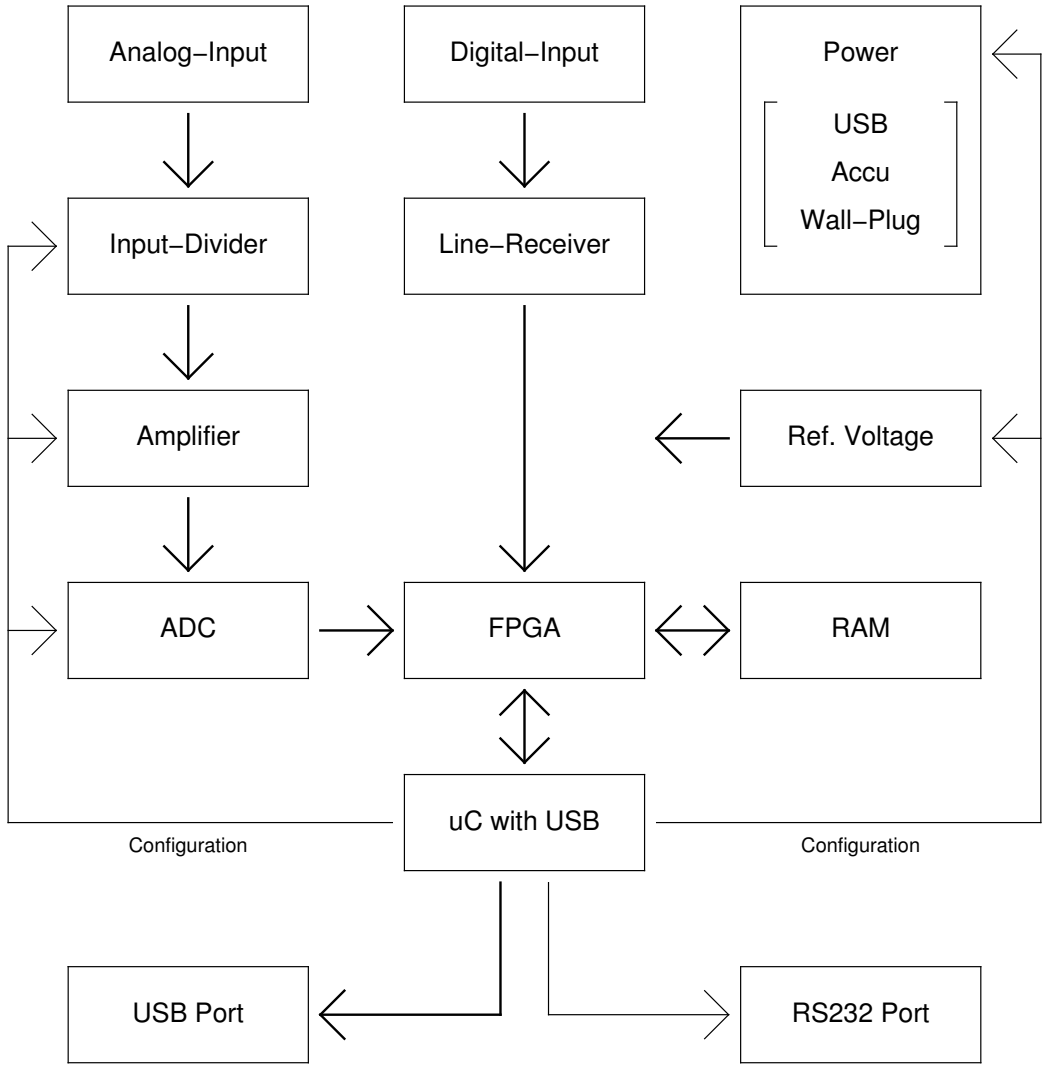
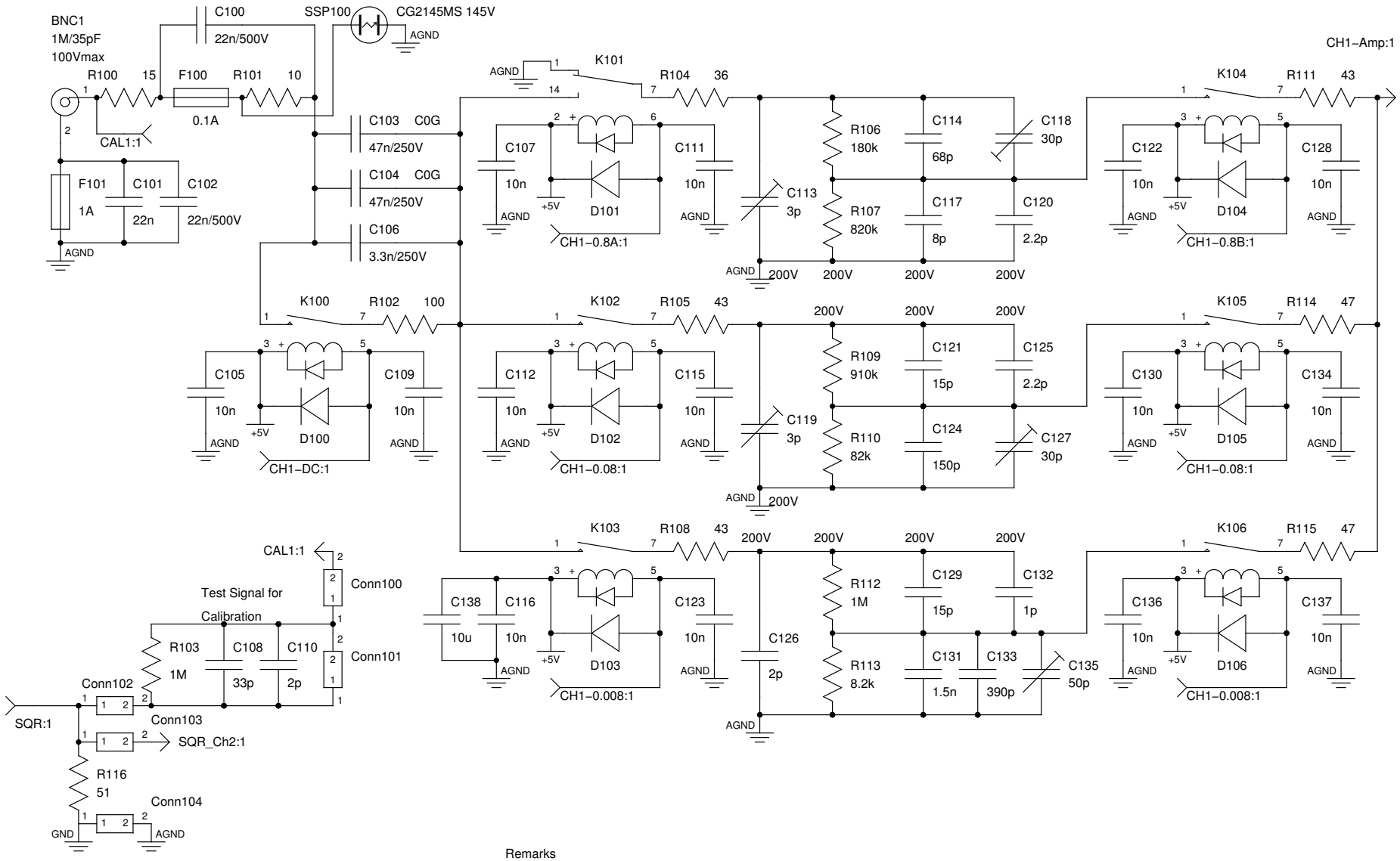
Data Acquisition Device –– Digital Storage Oscilloscope (PC–based)



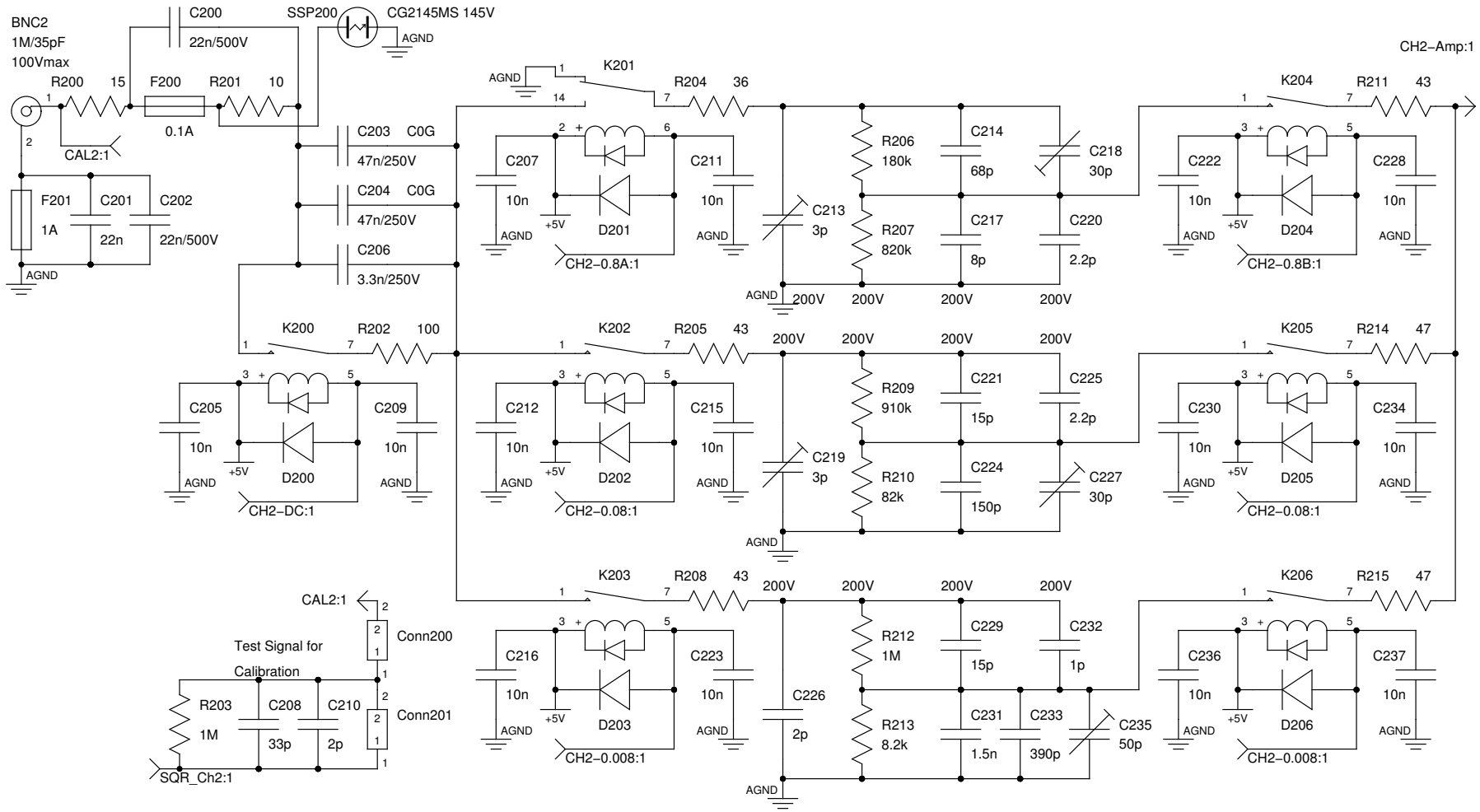
DAD/DSO, Overview	
File: Overview.sch	Sheet: 0 of 19
Author: S. Salewski	Rev: A 0.03
Copyright: All Rights Reserved	Date: 01–SEP–2008



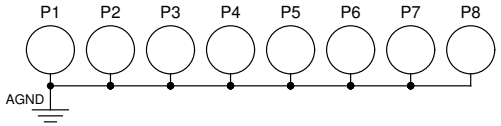
Remarks

- Flyback diodes are redundant
- 10n capacitors may be obsolete
- 47n/250V C0G should be fine –– no foil cap. necessary
- A 1.65V square signal is available for calibration
- Reed–Relays: Meder_SILxx–1A72–71D&Meder_DIPxx–1C90–51D
- Estimated Inductance of Reed Relays: 25nH –– series resistors are optimized for this value, fine tuning is necessary.

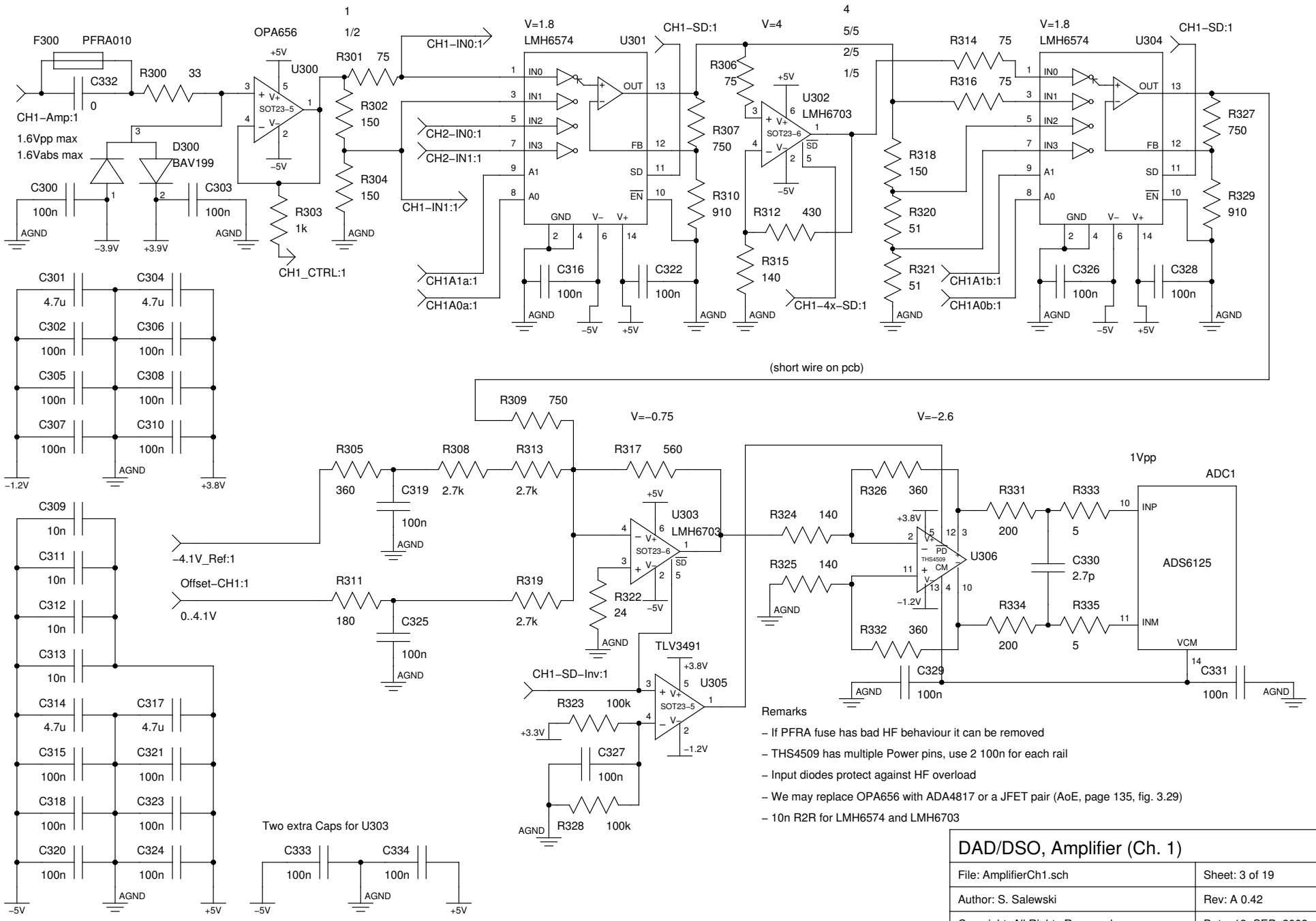
DAD/DSO, Input Divider (Ch. 1)	
File: InputDividerCh1.sch	Sheet: 1 of 19
Author: S. Salewski	Rev: A 0.43
Copyright: All Rights Reserved	Date: 21–SEP–2009



Soldering pads for mounting shielding box



DAD/DSO, Input Divider (Ch. 2)	
File: InputDividerCh2.sch	Sheet: 2 of 19
Author: S. Salewski	Rev: Copy of Sheet 1
Copyright: All Rights Reserved	Date: 01−SEP−2009



Remarks

– If PFRA fuse has bad HF behaviour it can be removed

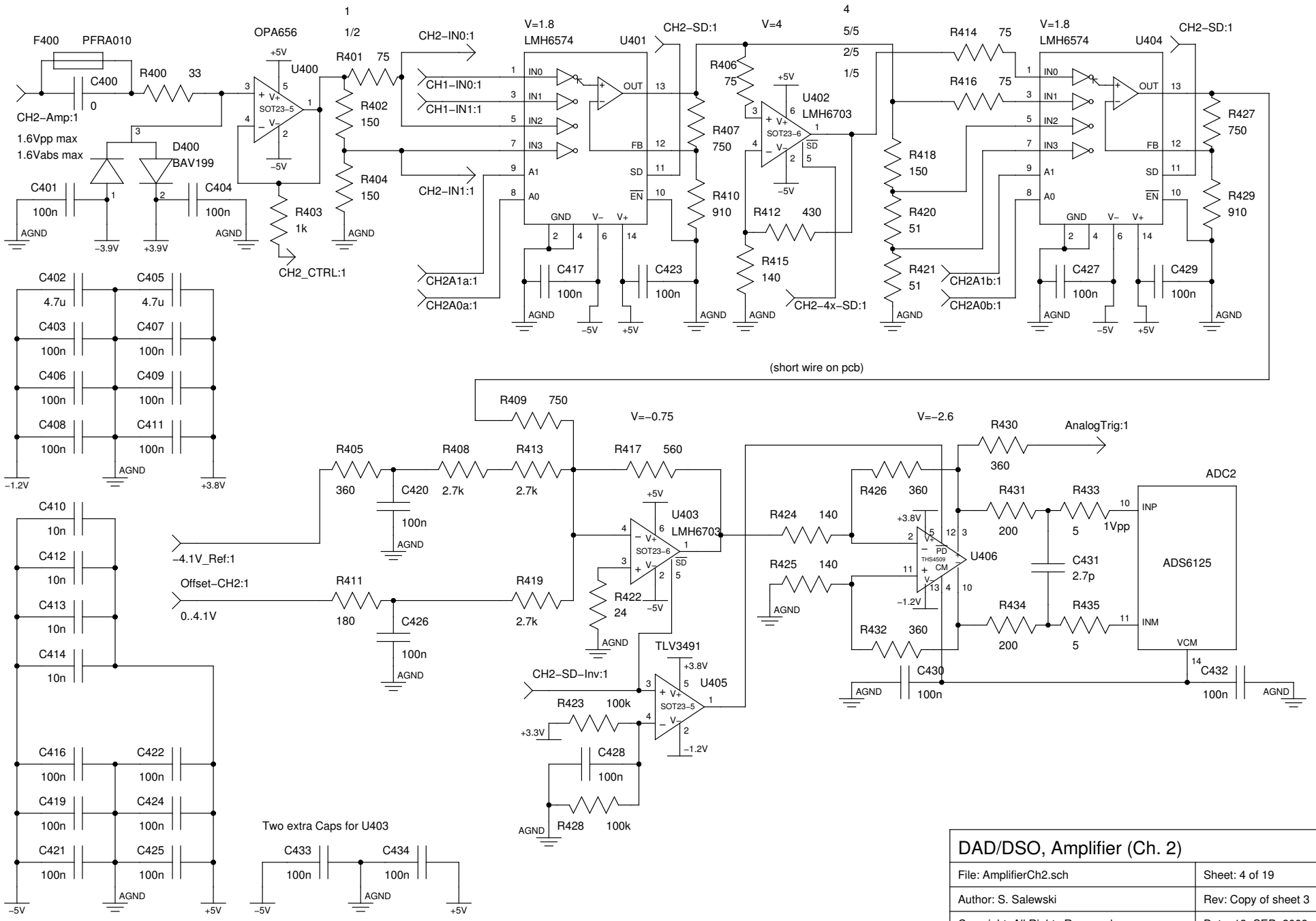
– THS4509 has multiple Power pins, use 2 100n for each rail

– Input diodes protect against HF overload

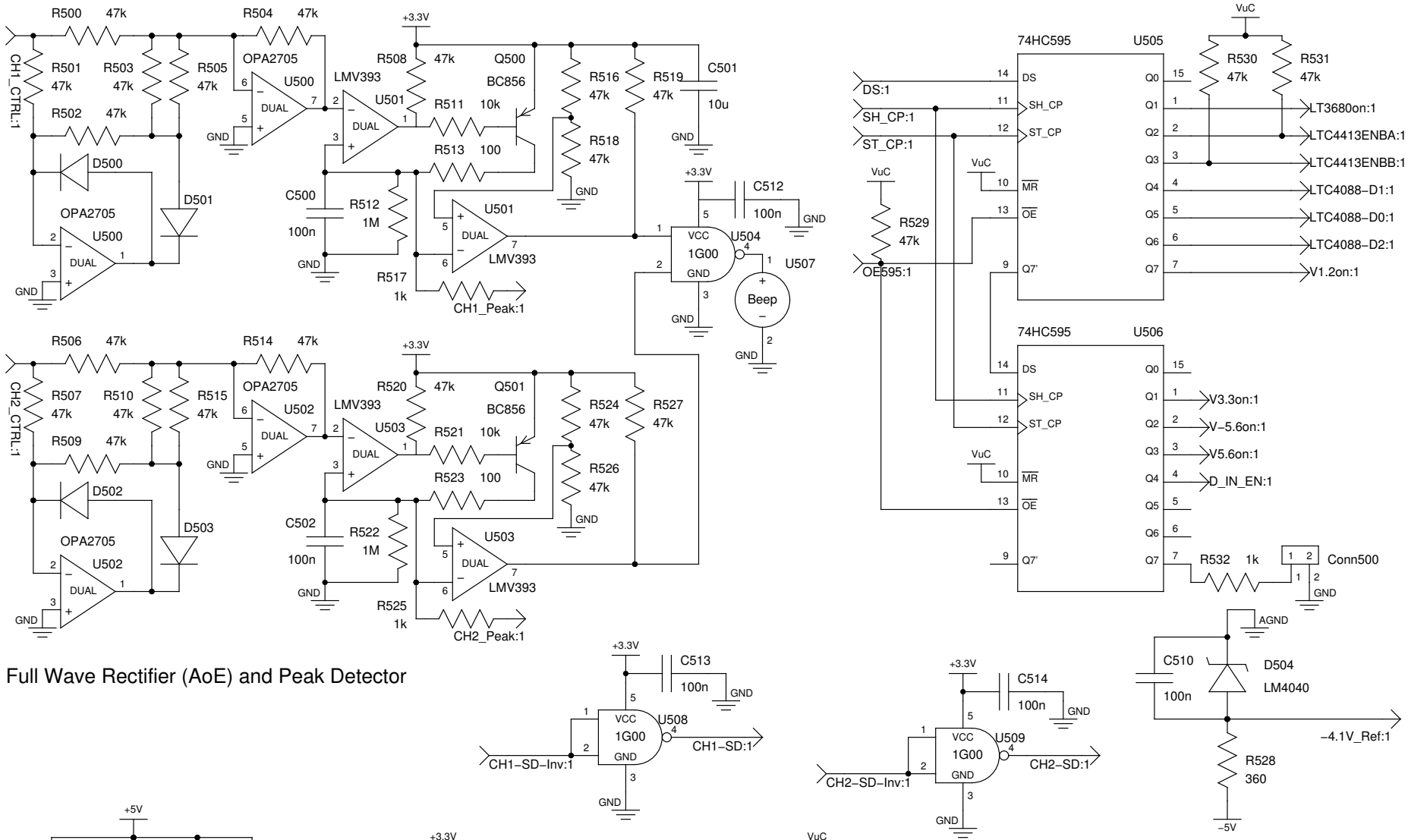
– We may replace OPA656 with ADA4817 or a JFET pair (AoE, page 135, fig. 3.29)

– 10n R2R for LMH6574 and LMH6703

DAD/DSO, Amplifier (Ch. 1)	
File: AmplifierCh1.sch	Sheet: 3 of 19
Author: S. Salewski	Rev: A 0.42
	Date: 18−SEP−2009

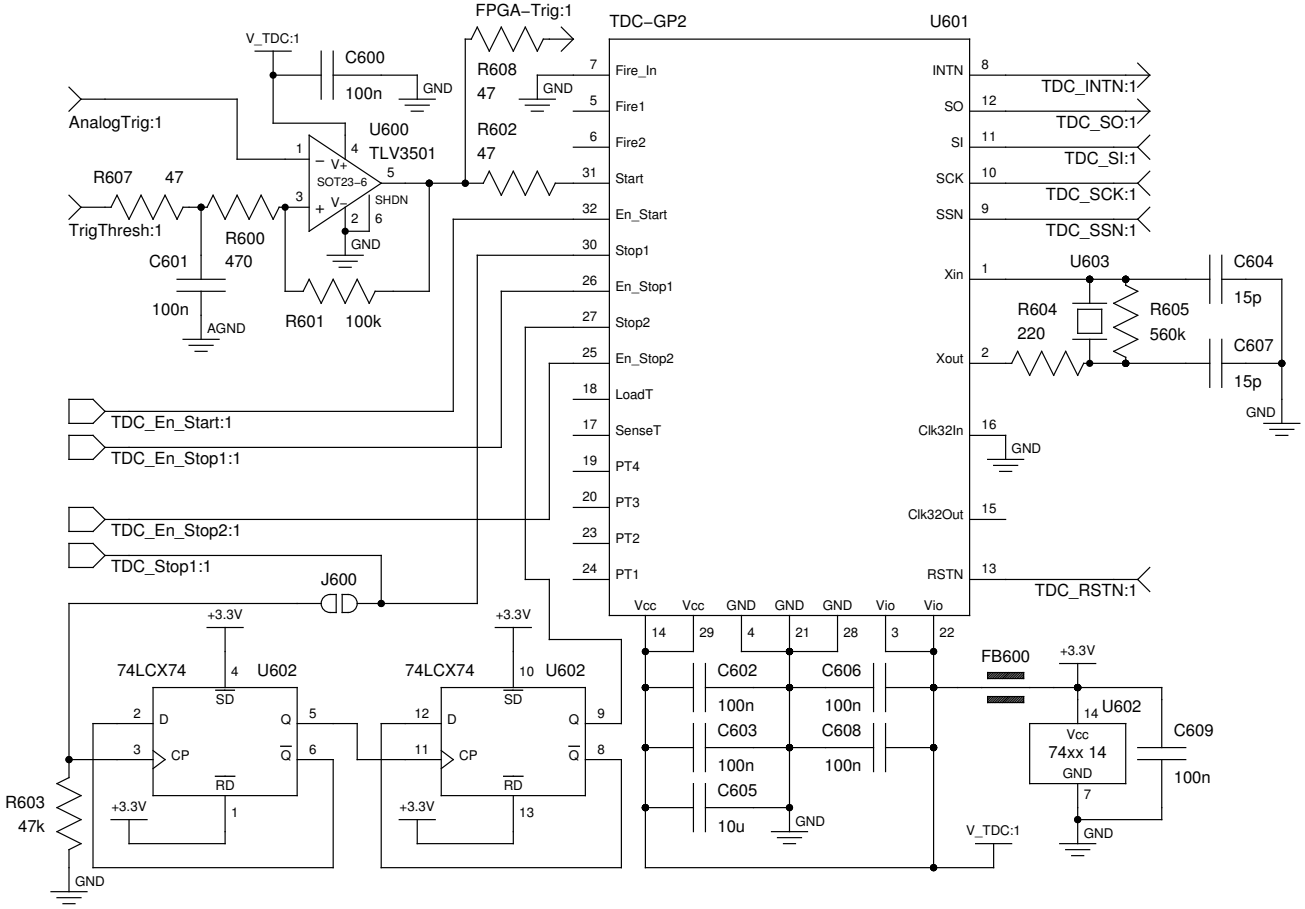


DAD/DSO, Amplifier (Ch. 2)	
File: AmplifierCh2.sch	Sheet: 4 of 19
Author: S. Salewski	Rev: Copy of sheet 3
Copyright: All Rights Reserved	Date: 18−SEP−2009



DAD/DSO, Amplifier Shared Parts	
File: AmpCommon.sch	Sheet: 5 of 19
Author: S. Salewski	Rev: A 0.26
	Date: 06−SEP−2009

Analog Trigger and TDC (Time to Digital Converter) for
Equivalent Time Sampling (ETS) also called
Random−Sampling or Postcorrelated Undersampling



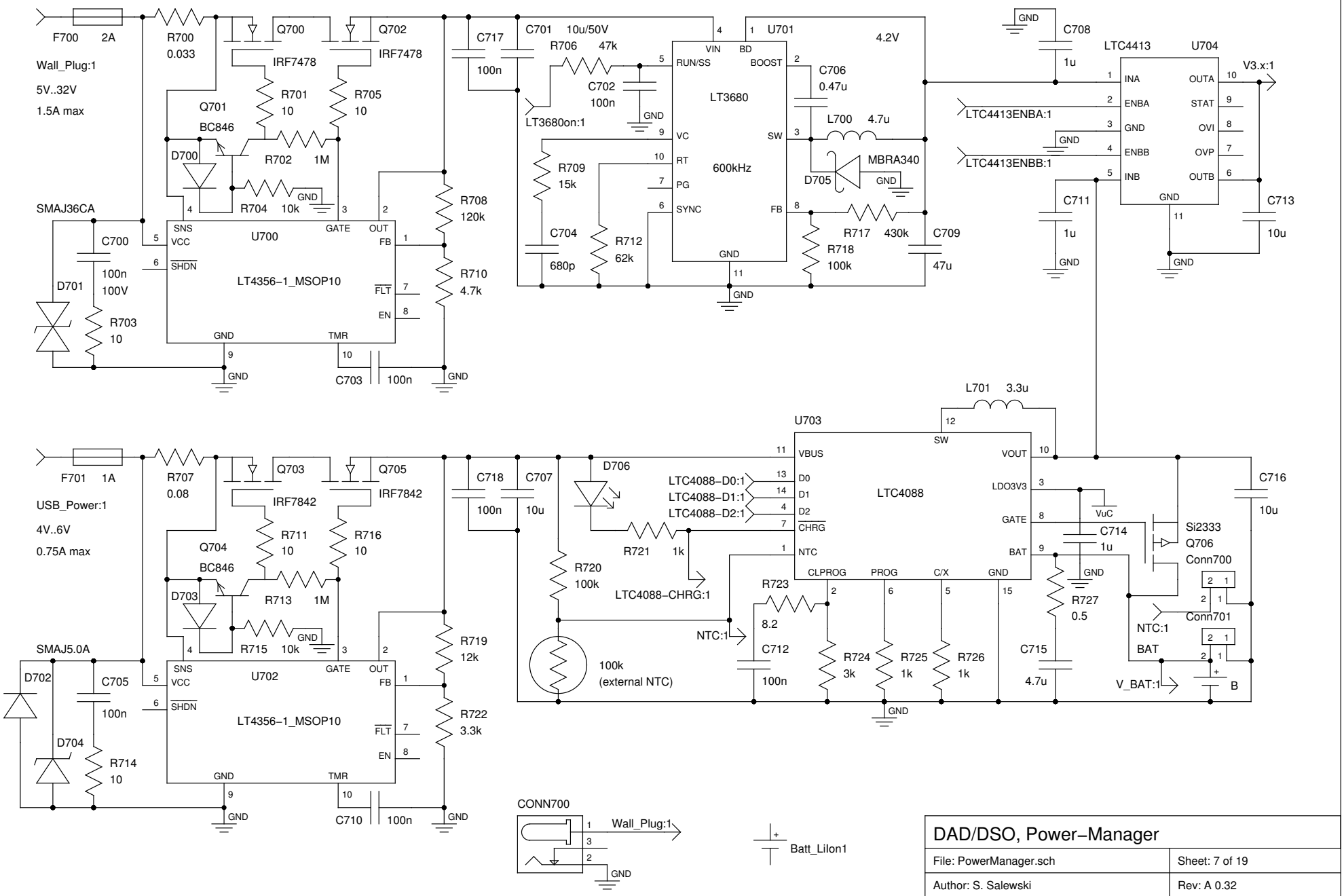
Remarks

– Clock Prescaler (FF) should be obsolete

– En_Start/En_Stop from FPGA

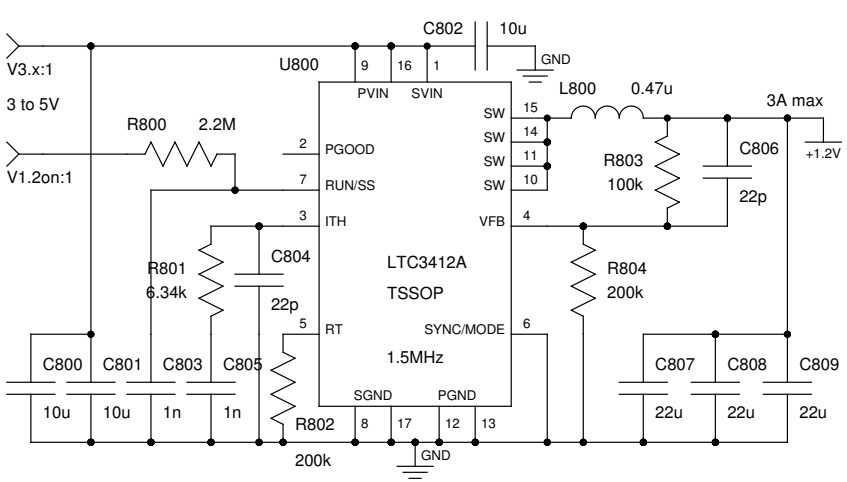
– Stop from ADC Clock Out

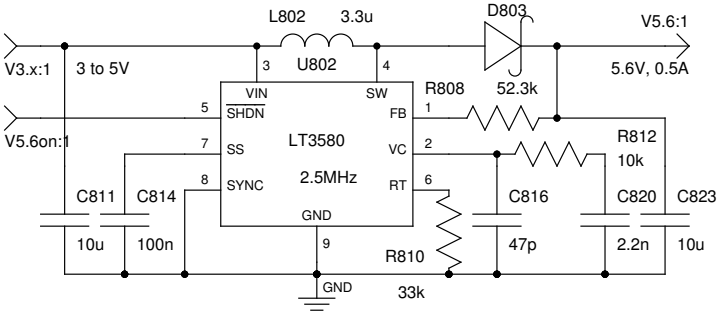
DAD/DSO, Analog Trigger & TDC	
File: TDC.sch	Sheet: 6 of 19
Author: S. Salewski	Rev: A 0.13
Copyright: All Rights Reserved	Date: 06−SEP−2009

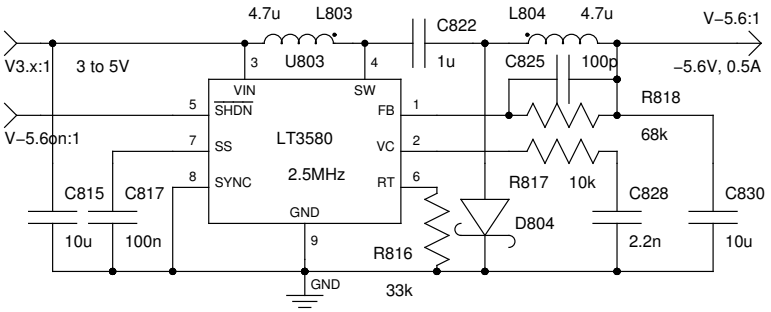


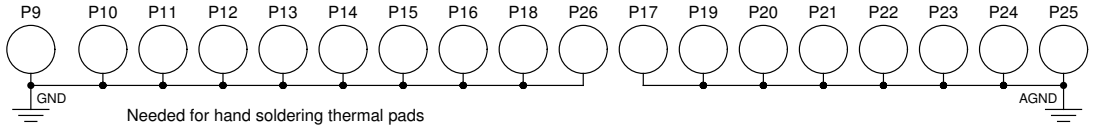
DAD/DSO, Power−Manager

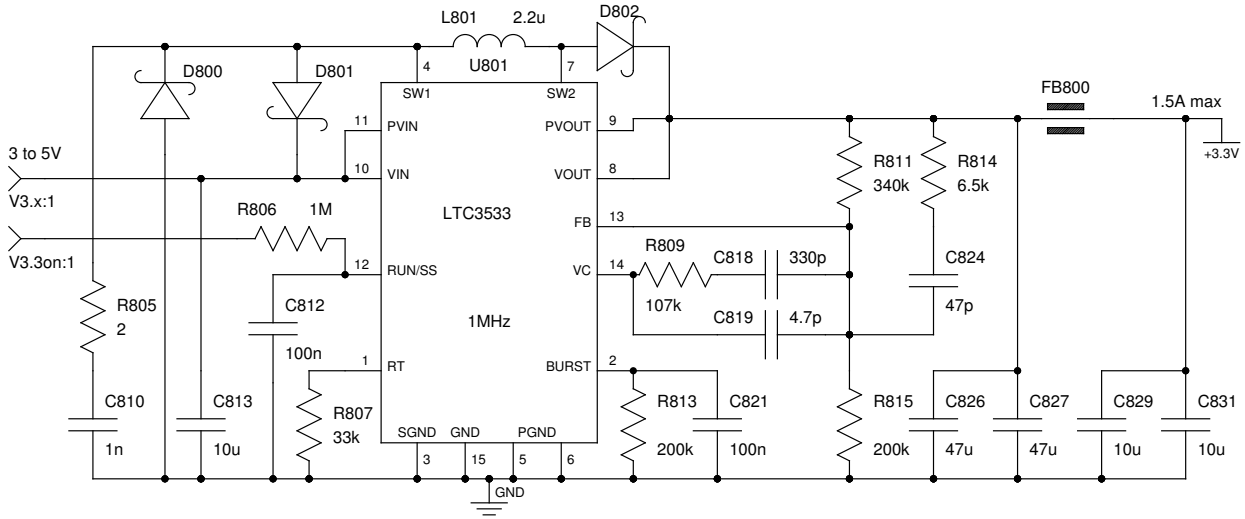
File: PowerManager.sch	Sheet: 7 of 19
Author: S. Salewski	Rev: A 0.32
Copyright: All Rights Reserved	Date: 21−SEP−2009

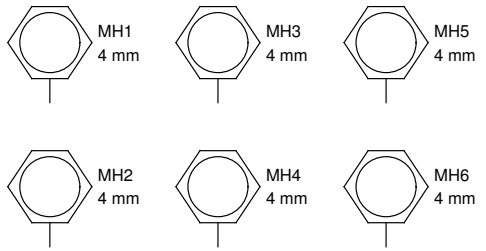






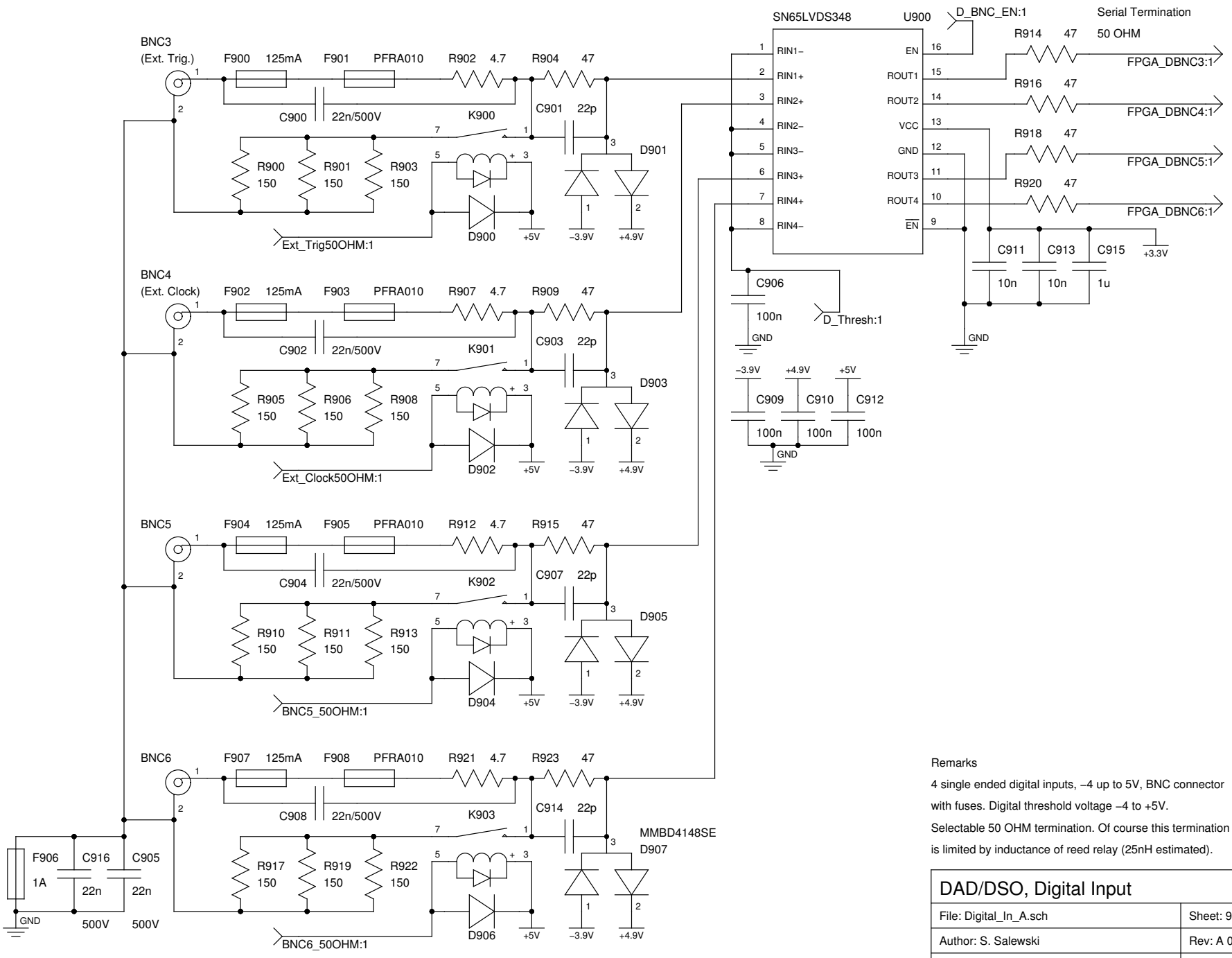






DAD/DSO, DC/DC Converters

File: DC_DC_Converter.sch	Sheet: 8 of 19
Author: S. Salewski	Rev: A 0.24
	Date: 21−SEP−2009

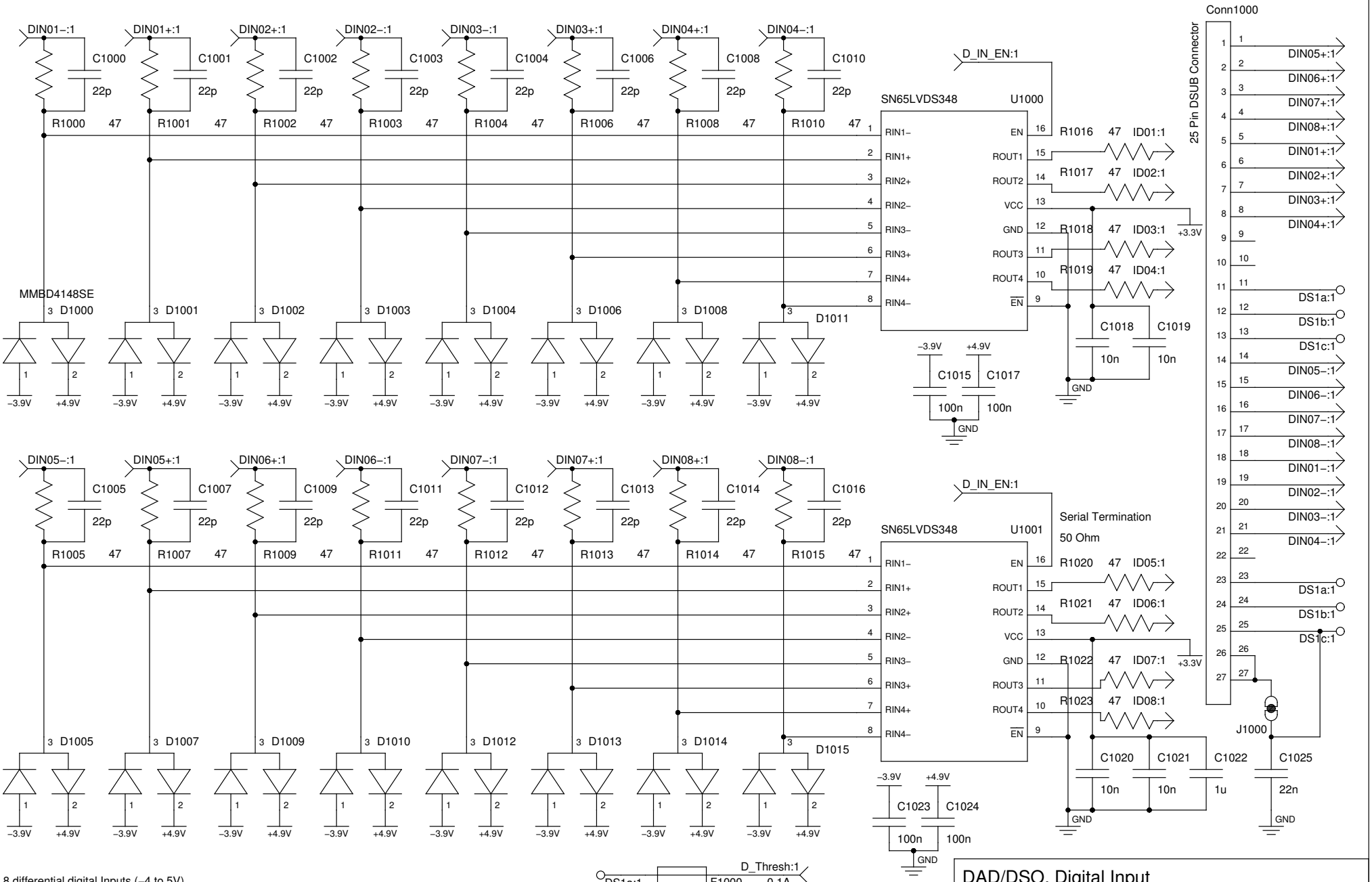


Remarks

4 single ended digital inputs, −4 up to 5V, BNC connector with fuses. Digital threshold voltage −4 to +5V.

Selectable 50 OHM termination. Of course this termination is limited by inductance of reed relay (25nH estimated).

DAD/DSO, Digital Input	
File: Digital_In_A.sch	Sheet: 9 of 19
Author: S. Salewski	Rev: A 0.18
Copyright: All Rights Reserved	Date: 16−AUG−2009



8 differential digital Inputs (–4 to 5V)

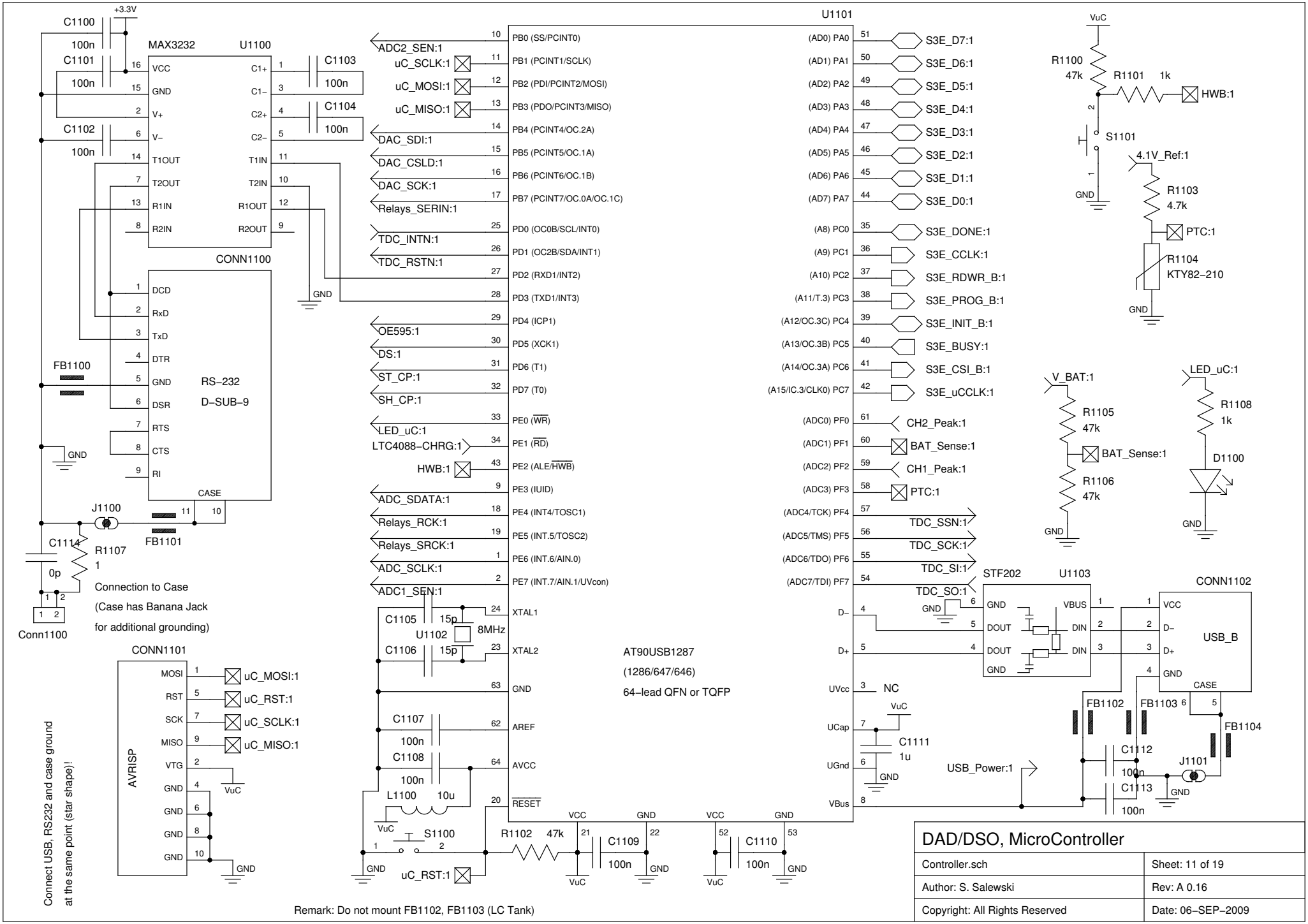
Terminating resistors can be mounted on a tiny external pcb board,

connected by a DSUB connector –– reference voltage can be connected

to all negativ inputs. This should make this input very flexible.

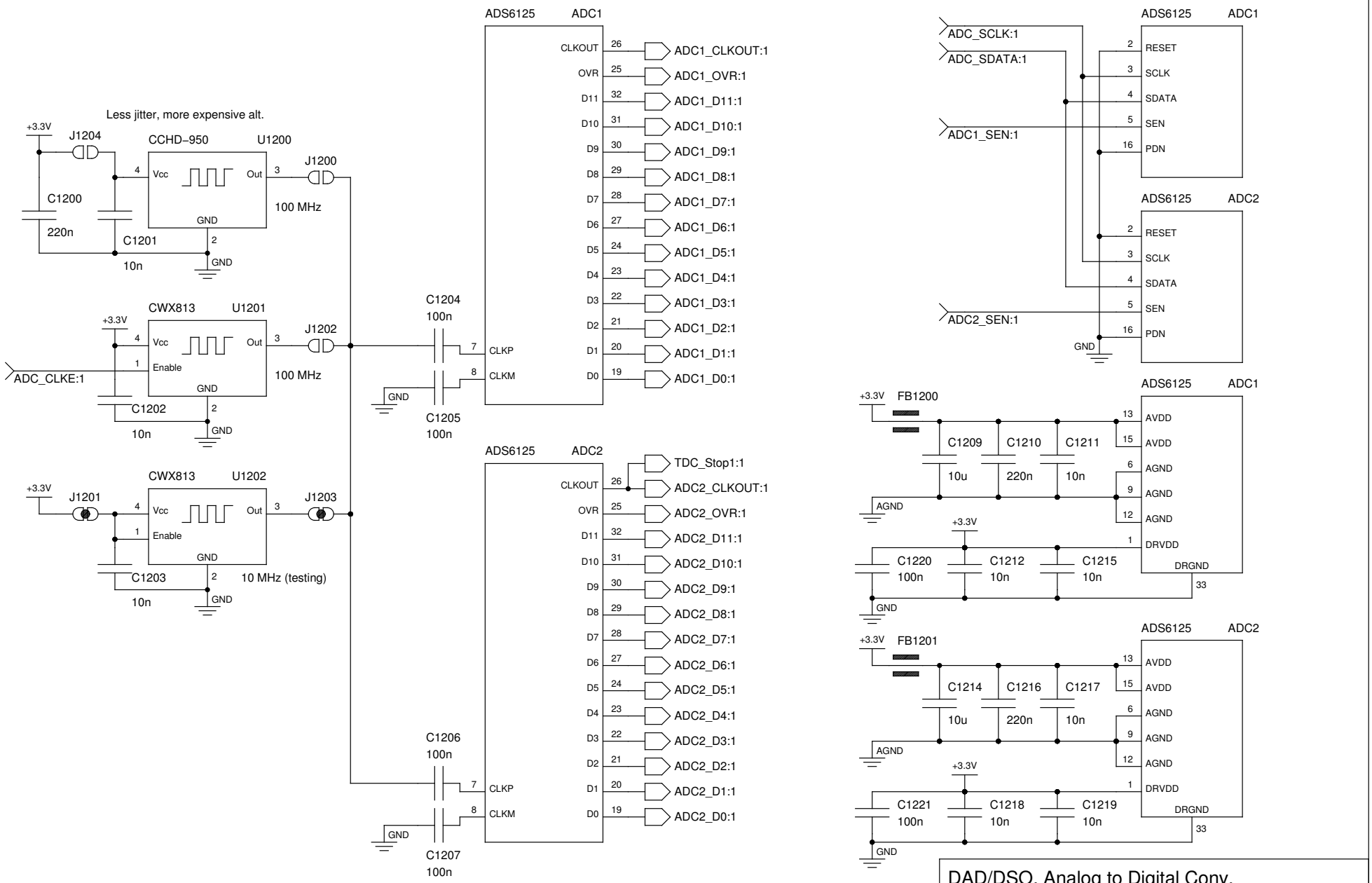
DAD/DSO, Digital Input

File: Digital_In_B.sch	Sheet: 10 of 19
Author: S. Salewski	Rev: A 0.20
Copyright: All Rights Reserved	Date: 19–AUG–2009



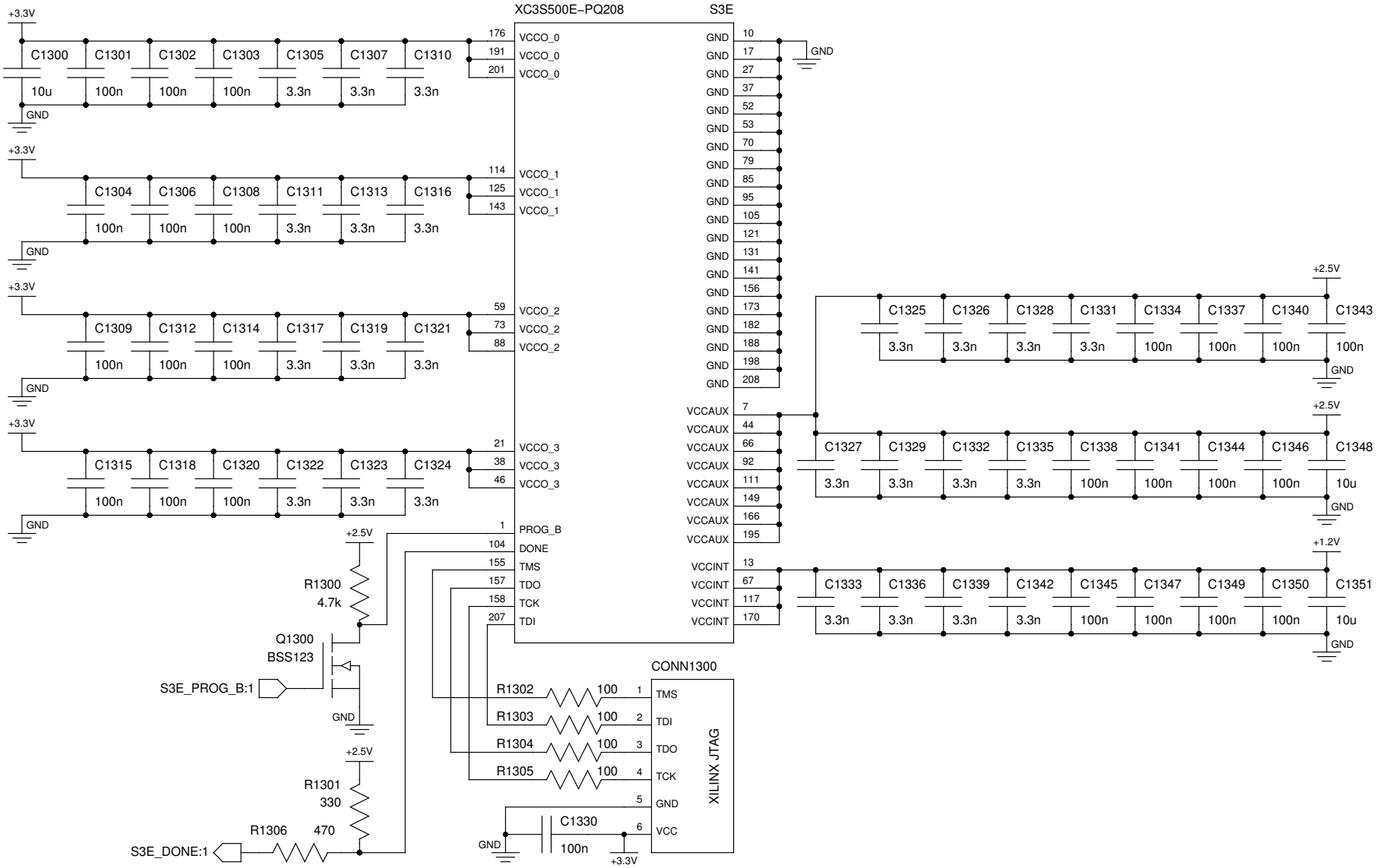
DAD/DSO, MicroController

Controller.sch	Sheet: 11 of 19
Author: S. Salewski	Rev: A 0.16
Copyright: All Rights Reserved	Date: 06−SEP−2009

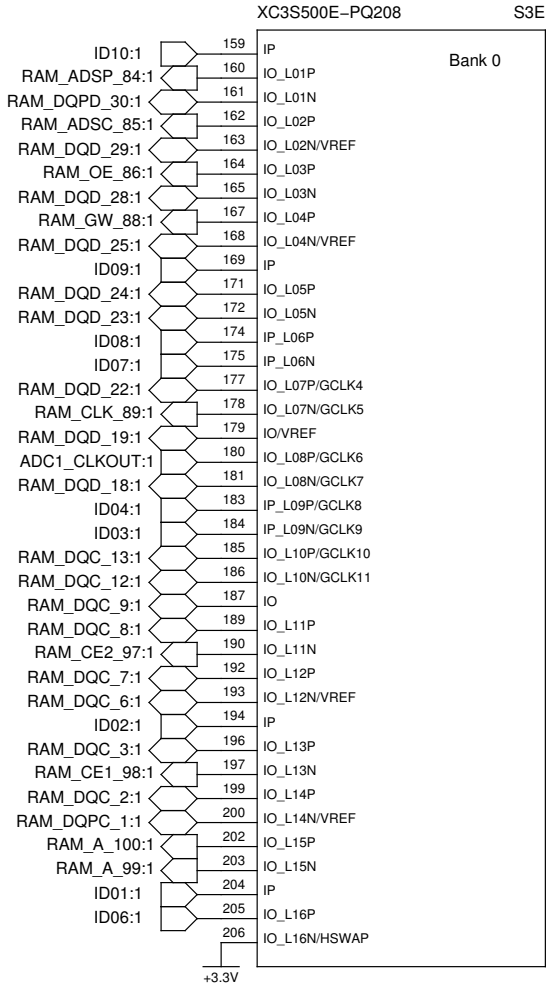


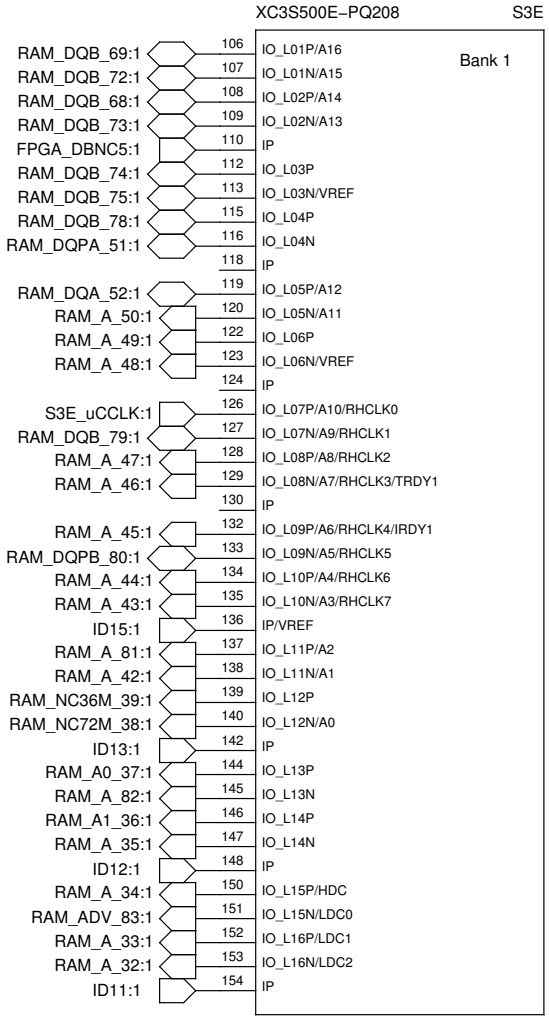
DAD/DSO, Analog to Digital Conv.

ADC.sch	Sheet: 12 of 19
Author: S. Salewski	Rev: A 0.14
	Date: 06–SEP–2009

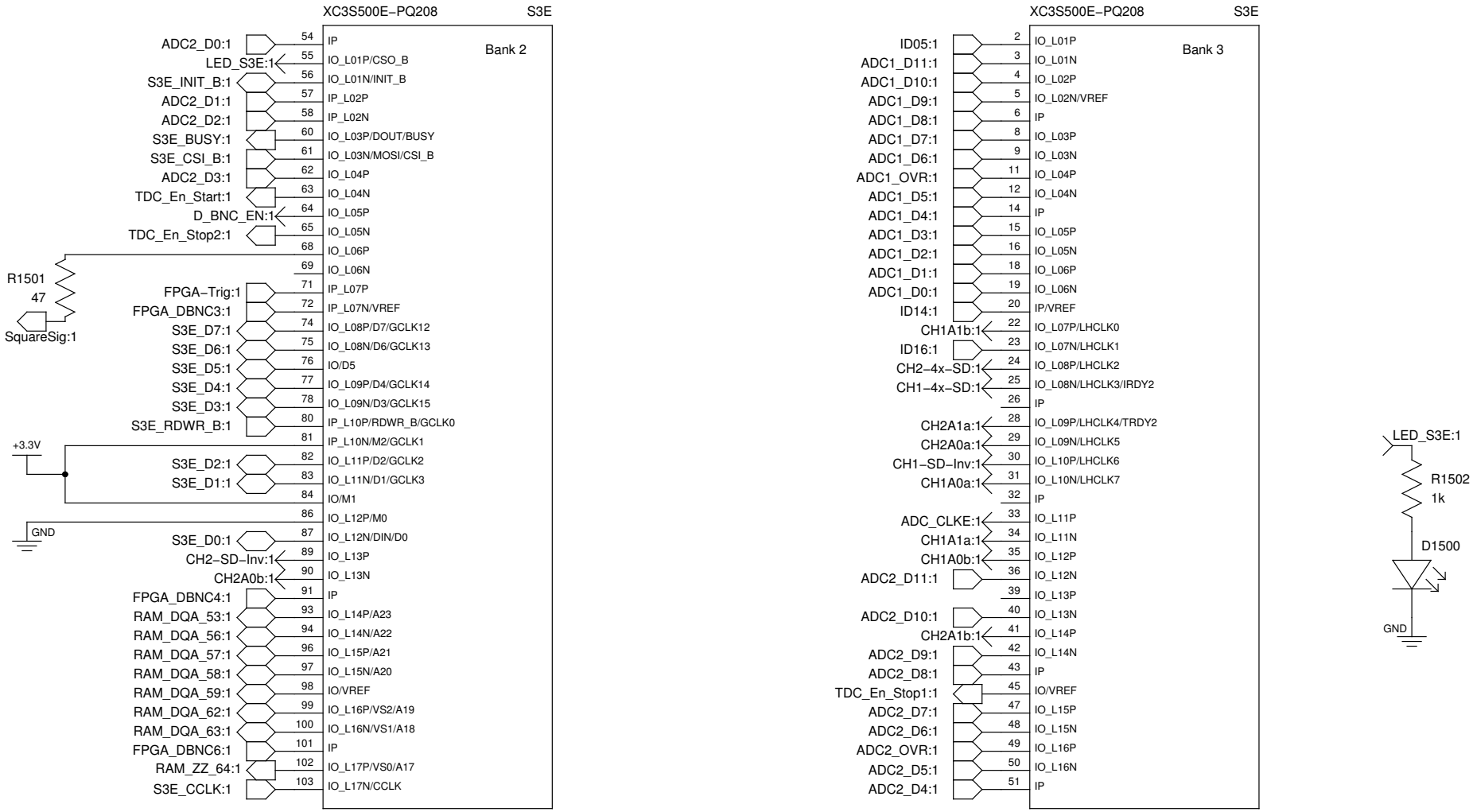


DAD/DSO, FPGA_Power	
FPGA_Power.sch	Sheet: 13 of 19
Author: S. Salewski	Rev: A 0.09
Copyright: All Rights Reserved	Date: 06−SEP−2009





DAD/DSO, FPGA B0,B1	
FPGA_B0B1.sch	Sheet: 14 of 19
Author: S. Salewski	Rev: A 0.12
	Date: 06−SEP−2009

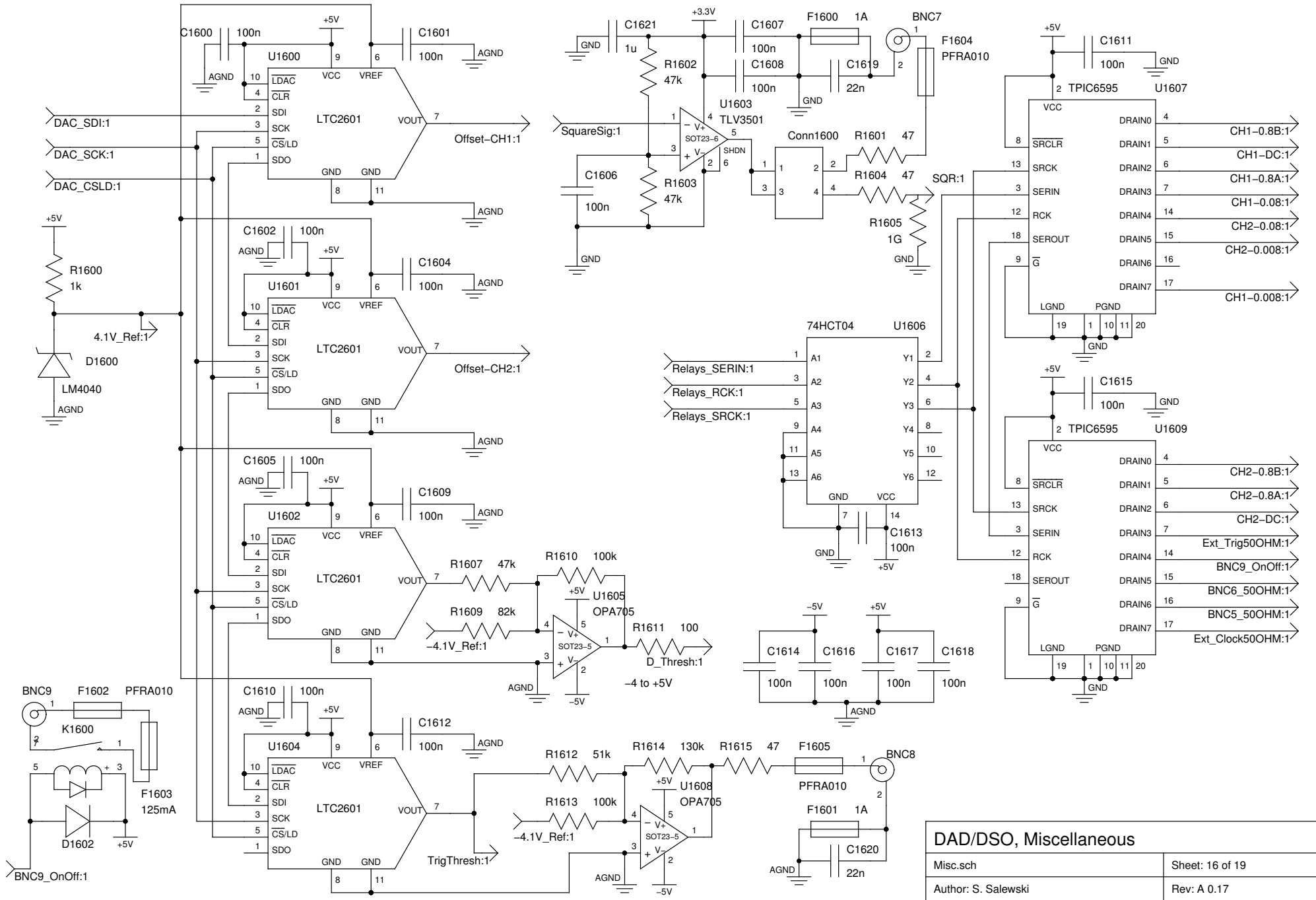


Remarks

− Signals with plain arrow symbol are low speed

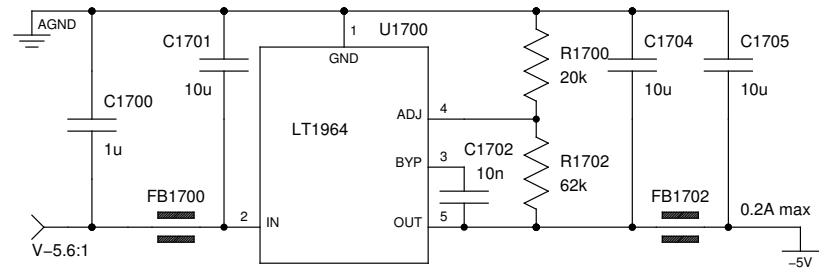
− CCLK, BUSY, RDWR, CSI and D[7:0] is used for communication with uC after configuration too!

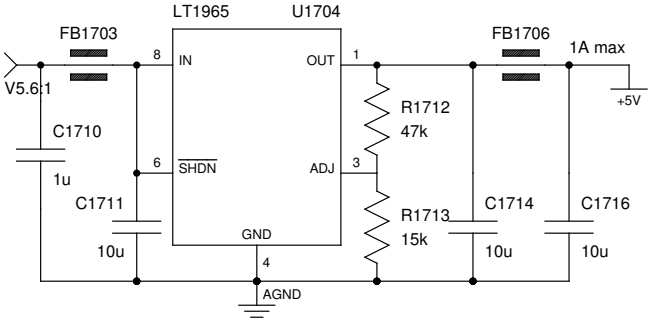
DAD/DSO, FPGA B2,B3	
FPGA_B2B3.sch	Sheet: 15 of 19
Author: S. Salewski	Rev: A 0.11
	Date: 06−SEP−2009

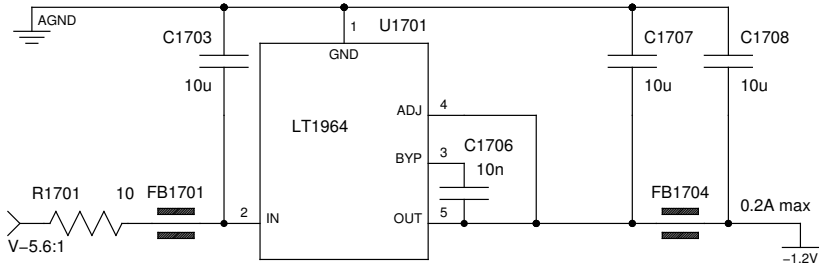


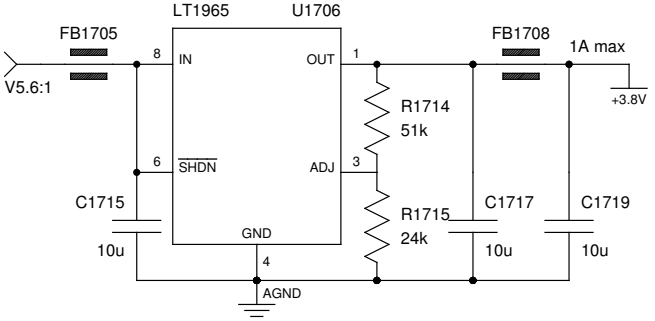
DAD/DSO, Miscellaneous

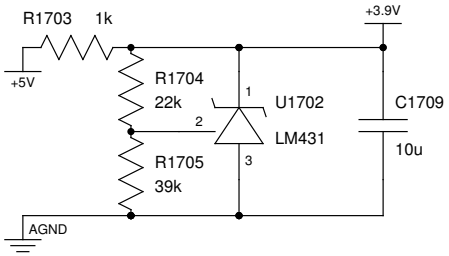
Misc.sch	Sheet: 16 of 19
Author: S. Salewski	Rev: A 0.17
	Date: 06−SEP−2009

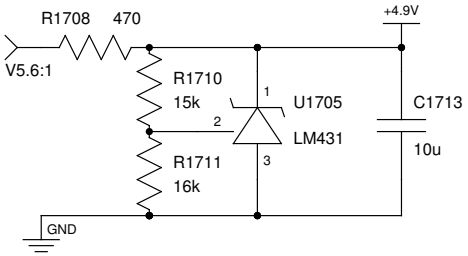


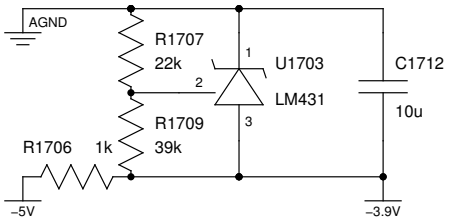


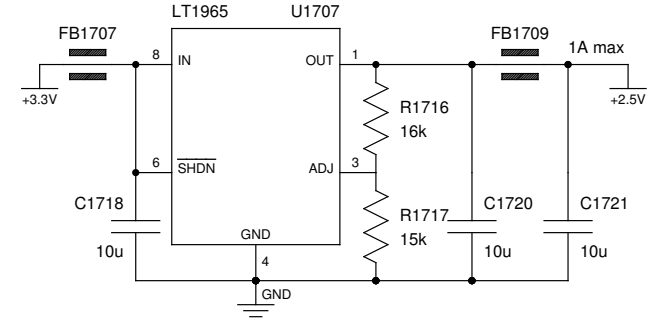








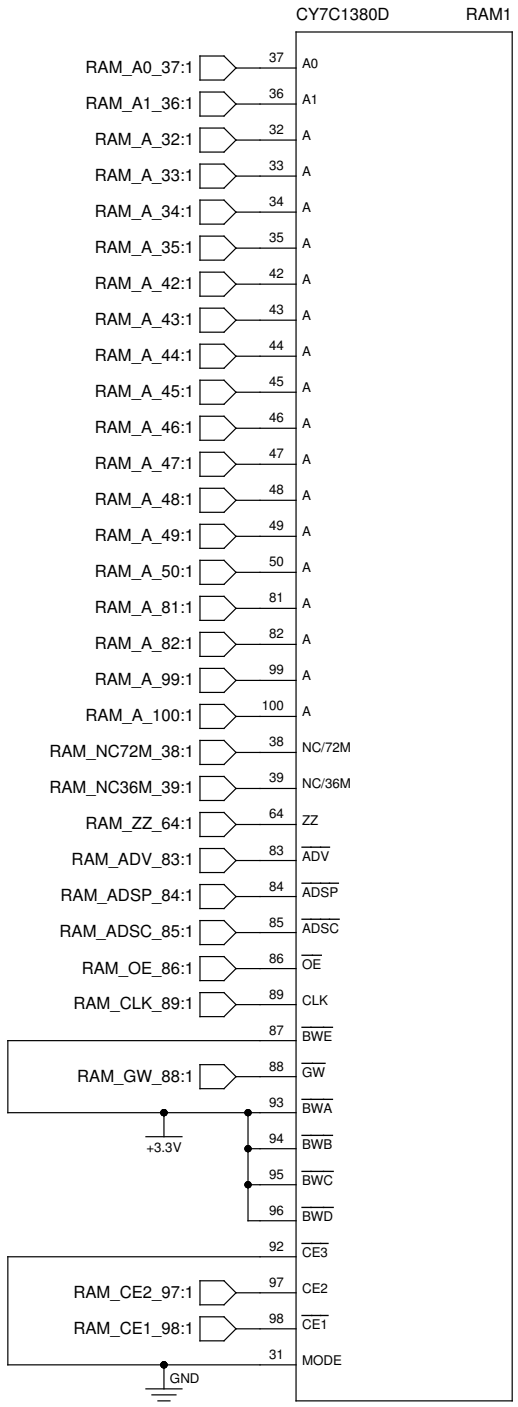


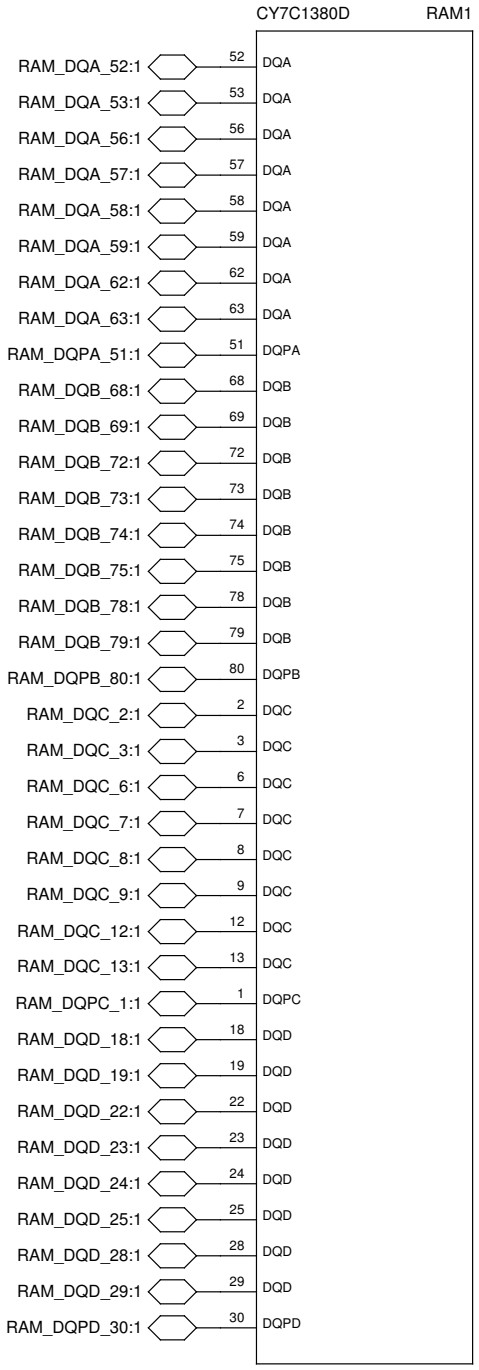


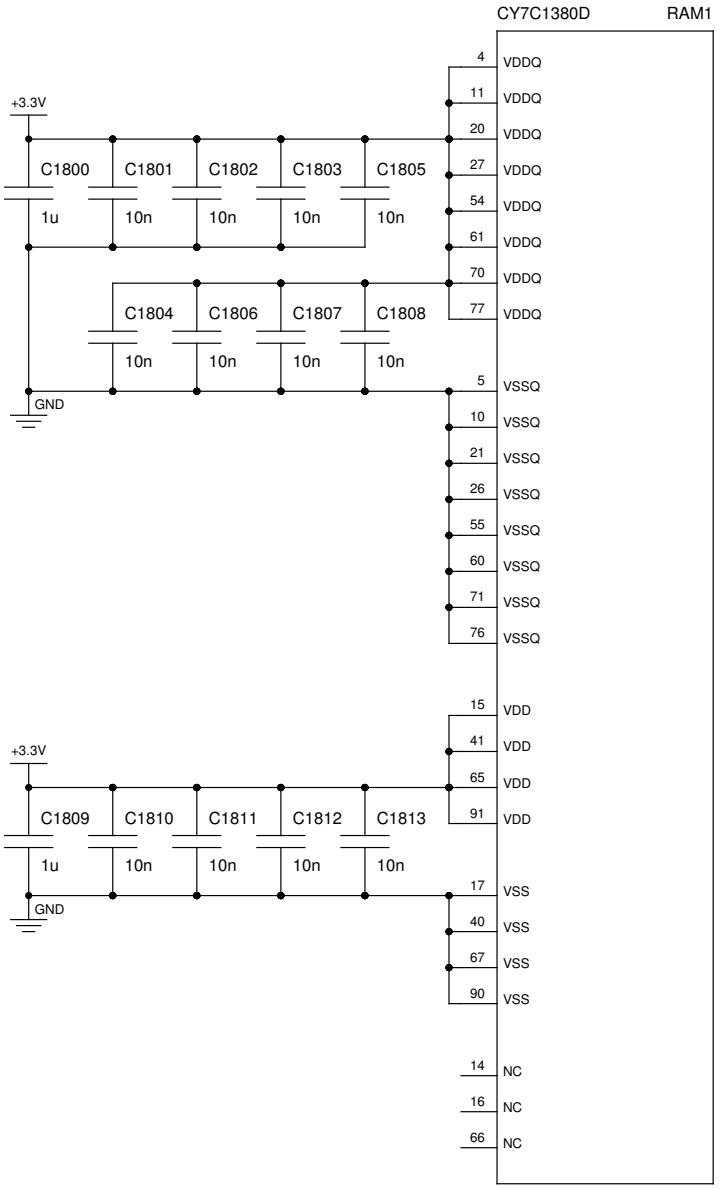
Remarks

− Voltages generated with LM431 are for Overvoltage Protection only −− they have to support reverse current

DAD/DSO, Linear Regulators	
File: Lin_Regulators.sch	Sheet: 17 of 19
Author: S. Salewski	Rev: A 0.10
	Date: 21−SEP−2009

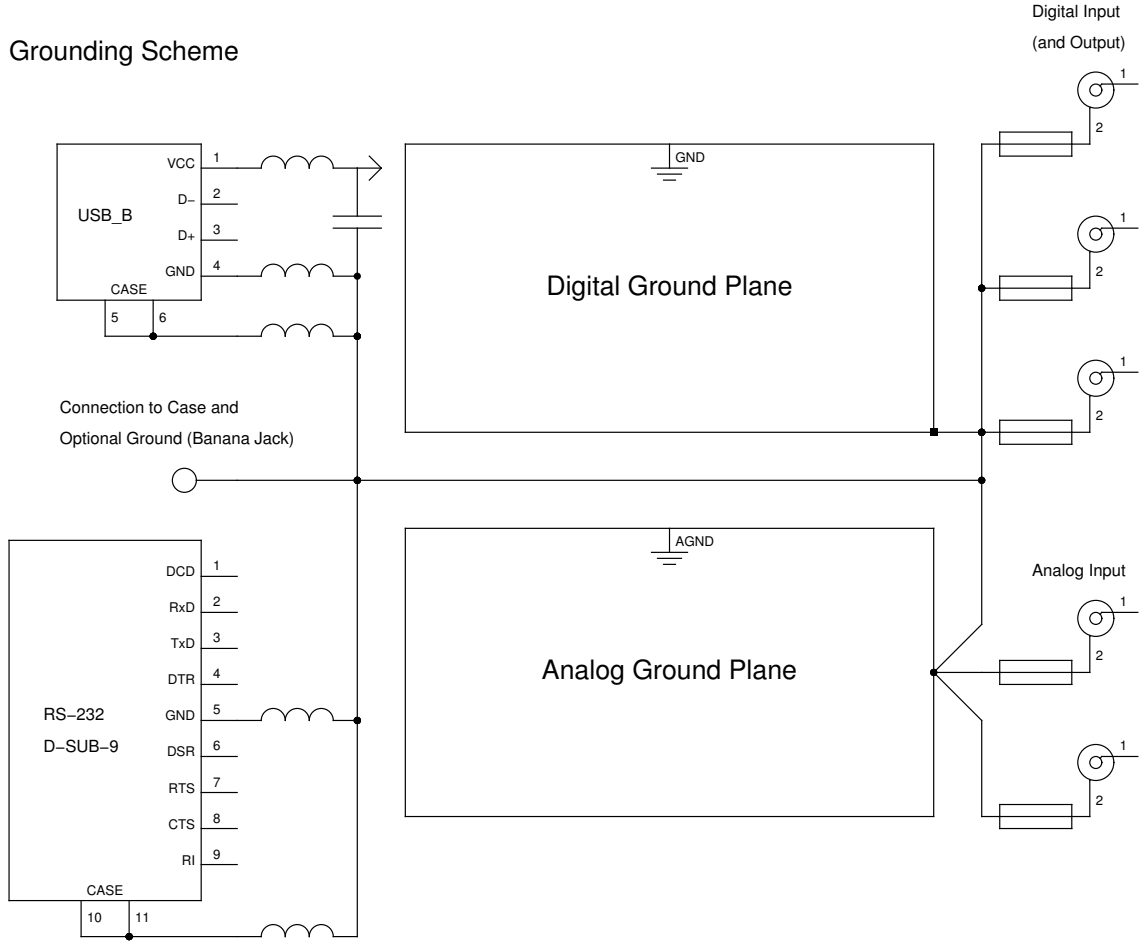






DAD/DSO, RAM Module	
RAM.sch	Sheet: 18 of 19
Author: S. Salewski	Rev: A 0.10
Copyright: All Rights Reserved	Date: 06–SEP–2009

Grounding Scheme



Remarks

– BNC connectors have no direct connection to Case

– Optional Fuses (1A, 0.2 OHM) will limit ground current to PC if BNC shield is connected to mains voltage (accident)

DAD/DSO, Grounding	
File: Grounding.sch	Sheet: Appendix A
Author: S. Salewski	Rev: A 0.01
	Date: 14–SEP–2008